THIS APPLICATION IS A CIP OF 10/154,577.
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AN INTEGRAL TOPSIDE VACUUM PACKAGE

Background

The invention relates to sealed vacuum packages and particularly to wafer pairs sealed having sealed chambers. More particularly, the invention relates to such packages having wafer topcaps.

The present application is a Continuation-in-Part of U.S. patent Application No. 10/154,577, filed on May 23, 2002, by B. Cole, R.A. Higashi et al., and entitled "Multi-Substrate Package Assembly."

Several patent documents may be related to sealed wafer pair chambers integrated vacuum packages. One patent document is U.S. Patent No. 5,895,233, issued April 20, 1999, to R. Higashi et al., and entitled "Integrated Silicon Micropackage for Infrared Devices," which is hereby incorporated by reference in the present specification. The assignee of this patent is the same assignee of the present invention. Another patent document is U.S. Patent No. 6,036,872, issued March 14, 2000, to R.A. Wood et al., and entitled "Method for Making a Wafer-Pair Having Sealed Chambers," which is hereby incorporated by reference in the present specification. The assignee of this patent document is the same assignee of the present invention.